REMARKS

Claims 1-8 and 12-23 remain pending in the application.

Claims 1-6, 17-19 and 22 over Persaud in view of Luan

Claims 1-6, 17-19 and 22 were rejected under 35 U.S.C. §103(a) as allegedly being obvious over Persaud et al., UK Patent Application No. GB2074762 ("Persaud") in view of Luan, U.S. Patent No. 5,911,149 ("Luan"). The Applicants respectfully traverse the rejection.

Claims 1-6, 17-19 and 22 recite a second agent receiving a clock signal from a first agent on a dedicated clock line, the second agent lacking a dedicated clock generator.

Persaud discloses a continuous 02 clock signal that is generated on each card (See page 3, lines 13-14). The continuous 02 signal from the master is distributed over the bus to all of the slave processors, together with a master clock signal (See Persaud, page 3, lines 15-17). A synchronizing circuit on each slave processor card operates on the continuous 02 signal generated by the slave, and the oscillator clock to synchronize the local 6875 clock generator so that it is in synchronism with a 6875 clock generator on the master card (See Persaud, col. 3, lines 17-19).

Thus, Persaud discloses sending a synchronizing signal from a master to a slave's local clock generator to synchronize operations between the master and the slave. Persaud fails to disclose a system in which a second agent receiving a clock signal from a first agent on a dedicated clock line, the second agent lacking a dedicated clock generator, as recited by claims 1-6, 17-19 and 22.

The Examiner acknowledges that Persaud fails to disclose use of synchronous memory (Office Action, page 5). The Examiner relies on Luan to allegedly make up for the deficiencies in Persaud to arrive at the claimed features. The Applicants respectfully disagree.

Thus, even if it were obvious to modify Persaud with the disclosure of Luan (which as discussed above it is not), at best the theoretical result would be a system in which agents each have a dedicated clock generator to access a

synchronous memory. Thus, Persaud modified by the disclosure of Luan would still fail to disclose or suggest a second agent receiving a clock signal from a first agent on a dedicated clock line, the second agent lacking a dedicated clock generator, as recited by claims 1-6, 17-19 and 22.

Moreover, "Teachings of references can be combined only if there is some suggestion or incentive to do so." In re Fine, 5 USPQ2d 1596,1600 (Fed. Cir. 1988) (quoting ACS Hosp. Sys. v. Montefiore Hosp., 221 USPQ 929, 933 (Fed. Cir. 1984)) (emphasis in original). The Examiner acknowledged that Persaud fails to disclose synchronous memory. However, neither Persaud nor Luan provide any motivation to completely redesign Persaud's system to include a synchronous memory, which could not simply be dropped in to replace the disclosed asynchronous memory. The inclusion of synchronous memory would not alleviate any disclosed shortcomings in Persaud to provide any new functionality. In fact, completely redesigning Persaud's system to replace the disclose asynchronous memory with synchronous memory would result in Persaud still solving the **same disclosed problem** of sharing a memory between a master and slave. Persaud modified by Luan would still fail to address timing issues that are addressed by Applicants' clock routing.

Moreover, the Examiner acknowledges that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references or in the knowledge generally available to one or ordinary skill in the art (See Office Action, page 16). The Examiner goes on to point out advantages of features of Luan's invention (See Office Action, page 16 and 17). However, it is the motivation to modify Persaud that is at issue, **NOT** why Luan uses components to perform Luan's invention. The Examiner has not provided motivation why one of ordinary skill in the art would take components from Luan and place them in Persaud's system that would **NOT** benefit Persaud's invention.

Accordingly, for at least all the above reasons, claims 1-6, 17-19 and 22 are patentable over the prior art of record. It is therefore respectfully requested that the rejection be withdrawn.

Claims 7, 8, 12, 20, 21 and 23 over Wu in view of Persaud and Persaud in view of Wu

Claims 7, 8 and 12 were rejected under 35 U.S.C. §103(a) as allegedly being obvious over Wu et al., U.S. Patent No. 5,659,715 ("Wu") in view of Persaud; claims 20 and 21 rejected under 35 U.S.C. §103(a) as allegedly being obvious over Persaud in view of Wu; and claim 23 was rejected under 35 U.S.C. §103(a) as allegedly being obvious over Wu. The Applicants respectfully traverse the rejection.

Claims 7, 8, 12, 20, 21 and 23 recite a second agent receiving a clock signal from a first agent on a dedicated clock line, the second agent lacking a dedicated clock generator.

As discussed above, Persaud fails to disclose or suggest a second agent receiving a clock signal from a first agent on a dedicated clock line, the second agent lacking a dedicated clock generator, as recited by claims 7,8, 12, 20, 21 and 23.

Wu appears to disclose a first and second processor having access to a common memory bank (See Fig. 3, items 302, 400 and 304 respectively). Address and data lines (See Wu, items 306 and 308) running to the common memory bank (See Wu, item 304) are routed through a single source, the graphics controller (See Wu, item 400). The CPU (See Wu, item 302) and the graphics controller are tied together to route data to the common memory (See Wu, Fig. 3). The common memory is connected to the graphics controller which is connected to the CPU (See Wu, Fig. 3). A clock synthesizer interface provides for programming of a programmable clock synthesizer (See Wu, col. 8, lines 39-43).

Wu discloses a system in which a CPU and a graphics controller utilize a common clock signal produced by a programmable clock synthesizer to access a common synchronous memory. Although Wu discloses two agents accessing a common synchronous memory, Wu does NOT disclose or suggest a second agent receiving a clock signal from a first agent on a dedicated clock line, much less a second agent receiving a clock signal from a first agent on a

dedicated clock line with the second agent lacking a dedicated clock generator, as recited by claims 7, 8, 12, 20, 21 and 23.

Neither Wu modified by the teachings of Persaud nor Persaud modified by the teachings of Wu disclose, teach or suggest a second agent receiving a clock signal from a first agent on a dedicated clock line, the second agent lacking a dedicated clock generator, as recited by claims 7, 8, 12, 20, 21 and 23.

At best, even if the combination of Wu and Persaud were obvious, which it is not, the theoretical combination would result in a system and method of using a CPU and graphics controller for accessing a common memory. A programmable clock synthesizer would provide a clock signal to ALL the CPU, graphics controller and memory within the system. The CPU would additionally send synchronization to the graphics controller, which would be nonsensical since the graphics controller is already receiving a clock signal. Thus, even the theoretical combination fails to disclose or suggest a second agent receiving a clock signal from a first agent on a dedicated clock line, the second agent lacking a dedicated clock generator, as recited by claims 7, 8, 12, 20, 21 and 23.

Accordingly, for at least all the above reasons, claims 7, 8, 12, 20, 21 and 23 are patentable over the prior art of record. It is therefore respectfully requested that the rejection be withdrawn.

Claims 13-16 over Persaud in view of Muthal

Claims 13-16 were rejected under 35 U.S.C. §103(a) as allegedly being obvious over Persaud in view of Muthal, U.S. Patent No. 5,815,167 ("Muthal"). The Applicants respectfully traverse the rejection.

Claims 13-16 recite a second agent receiving a clock signal from a first agent on a dedicated clock line, the second agent lacking a dedicated clock generator.

As discussed above, Persaud fails to disclose or suggest a second agent receiving a clock signal from a first agent on a dedicated clock line, the second agent lacking a dedicated clock generator, as recited by claims 13-16.

The Office Action relies on Muthal to allegedly make up for the deficiencies in Persaud to arrive at the claimed invention. The Applicants respectfully disagree.

Muthal appears to disclose a computer system comprising a graphics controller, a memory controller and shared memory (See Abstract). The shared memory is accessible by both the memory controller and graphics controller (See Muthal, Abstract). Concurrent access to portions of the shared memory is given to the graphics controller and the memory controller (See Muthal, Abstract).

Although Muthal discloses a first and second agent accessing different portions of a shared non-dedicted memory memory simultaneously, Muthal fails to disclose how access to the shared portion of the memory system is synchronized between the processor and the graphics controller. Muthal makes **no mention** of how clock signals are routed throughout the system, much less disclose or suggest a second agent receiving a clock signal from a first agent on a dedicated clock line, the second agent lacking a dedicated clock generator, as recited by claims 13-16.

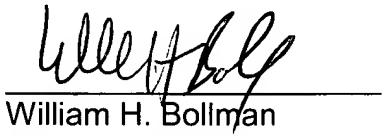
Thus, Persaud modified by the disclosure of Muthal would still fail to disclose, teach or **suggest** a second agent receiving a clock signal from a first agent on a dedicated clock line, the second agent lacking a dedicated clock generator, as recited by claims 13-16.

Accordingly, for at least all the above reasons, claims 13-16 are patentable over the prior art of record. It is therefore respectfully requested that the rejection be withdrawn.

Conclusion

All objections and rejections having been addressed, it is respectfully submitted that the subject application is in condition for allowance and a Notice to that effect is earnestly solicited.

Respectfully submitted,



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